Remarks/Arguments

Summary

By this amendment, claims 1, 4, 5, 8, 11, 12, 15, 18, and 19 were amended; claims 3, 10, and 17 were cancelled; and claims 22-25 were added. In addition, drawing 3A was amended. Accordingly, claims 1-2, 5-9, 11-16, and 18-25 are now pending in this application.

Drawings

Drawing 3A was amended to include the legend "Prior Art".

Claim Rejections – 35 U.S.C. §103

In the Office Action dated October 24, 2005 (hereafter, the Office Action), claims 1-21 were rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,414,904 to So et al. (hereafter So). Without acquiescing to the examiner's reasoning, the claims have been amended to obviate the rejections. In addition, Applicants respectfully submit the following comments regarding the patentability of now pending claims 1-2, 5-9, 11-16, and 18-25.

In the Office Action, the Examiner stated that elements 12a and 12b in Fig. 1 of So constitute a first memory module group and elements 12c and 12d in Fig. 1 of So constitute a second memory module group. In addition, the Examiner stated that elements DB1 through DB8 each constitute a system data bus. However, in a lengthy phone conversation on November 22, 2005, the Examiner changed his position regarding both the memory module groups and the system data buses. The Examiner now claims that elements 12a and 12c constitute a first memory module group and elements 12b and 12d constitute a second memory module group. The Examiner also claims that elements DB1 through DB4 collectively constitute a first system data bus and elements DB5 through DB8 collectively constitute a second system data bus.

The reasons for the Examiner's changed positions are as follows. First, if elements 12a and 12b belonged to the same memory module group, then both elements in the memory module group would be connected to the *same* system data bus rather than *different* system data buses as previously recited in claim 1. Accordingly, the Examiner now claims that elements 12a and 12c are connected to respectively *different* system buses. Second, if elements DB1 through DB8 each constituted system data buses, the number of system buses would be much larger than the number of modules in each memory module group. Accordingly, the Examiner now maintains that Fig. 1 of So contains two memory module groups and two system data buses.

Under either the Examiner's current or previous position, So fails to disclose that the system data buses are wired so that data transmission times between the memory modules in the first or second memory module group and the memory controller are the same. (See, for example, amended independent claims 1, 8, and 15). The Office Action claims on page 3, lines 9-14, that it would be obvious to wire elements DB1 through DB8 so that data transmission times between elements 12a and 12c and memory controller 11 are the same, and data transmission times between elements 12b and 12d and memory controller 11 are the same. Unfortunately, however, the Examiner offers only misplaced and fallacious arguments in support of this position.

For example, the Office Action refers to elements 20a through 20d in Fig. 2 of So as "memory modules", erroneously equating them with so-called "memory modules" 12a through 12d. The Office Action then goes on to allege that because elements 20a through 20d are "sequentially operated at uniform time intervals" (See, Office Action, page 3, line 13), "one of ordinary skill in the art *would have known* how to wire" (emphasis added) the system buses such that the data transmission times between the memory modules within a memory module group and the memory controller were the same. This argument has at least three fatal flaws. First, elements 20a through 20d are different from elements 12a through

12d. In fact, these elements are illustrated as internal, one bit elements formed within elements 12a through 12d. Accordingly, the timing of elements 20a through 20d says nothing of the data transmission times between elements 12a through 12d and memory controller 11, much less their *relative* data transmission times. Second, So's description of the timing of elements 20a through 20d as "sequential" and "uniform" refers to their relative input/output timing. (See, So at column 4, lines 50-65). Again, this says nothing of their transmission times. Finally, as the phrase "would have known how to wire" clearly indicates, the argument relies on impermissible hindsight. (See, MPEP 2141 II(C)). In other words, the argument simply tries to state what one of ordinary skill would be capable of implementing given foreknowledge of the claimed invention.

To formulate a proper rejection of the now pending claims under 35 U.S.C. §103, the Examiner would have to show at least the following three elements for each claim: (1) there is a suggestion or motivation, either in a reference(s) or in the knowledge of one skilled in the art, to modify the reference(s) or combine reference teachings; (2) there must be a reasonable expectation of success; and (3) the combined reference teachings must teach or suggest all claim limitations. (See, MPEP 2142). In addition, the suggestion to modify or combine teachings and the expectation of success would have to be found in the prior art and not in the applicant's disclosure. Id. Based on at least the foregoing explanation, the Office Action fails to meet these three required elements for independent claims 1, 8, and 15.

First, regarding element (1), the only alleged motivation presented in the Office Action to modify So relies on an erroneous interpretation of So's teachings and impermissible hindsight. Second, regarding element (2), the Office Action's suggestion to somehow modify the relative timing of elements 20a through 20d to achieve uniform data transmission times for memory modules would no doubt fail since the relative timing of elements 20a through 20d has little, if anything to do with the relative data transmission times of elements 12a through 12d. Finally,

regarding element (3), So fails to discuss the transmission times of elements 12a through 12d at all. Since the Office Action fails to meet *any* of the required elements for a rejection under 35 U.S.C. §103(a), independent claims 1, 8, and 15 should be allowed over So.

In the Office Action of October 24, 2005, the Examiner completely failed to address the merits of claims 4-7, 11-14, and 18-21. In addition, the Examiner failed to address the merits of various elements of independent claims 8 and 15. In particular, the Examiner failed to show where So discloses "a second memory module group having at least one memory module connected to all of the *N* system data buses" as recited in claim 8, or "each of the *N* system data buses including a plurality of data buffers" as recited in claim 15.

Regarding claims 4-7, 11-14, and 18-21, So fails to disclose the memory banks defined in claims 4-6, 11-13, and 18-20, or the relationship between the number of memory devices and bus width defined in claims 7, 14, and 21. In fact, the memory module 12 shown in Fig. 2 of So, simply shows a row of apparently 1-bit memory devices. Clearly, this is different from the "two or more banks" disclosed, for example, in claim 4. Moreover, So also fails to disclose chip select signals corresponding to the different banks as defined, for example, in claims 4, 11, and 18. Absent the various required disclosures, the rejection of claims 4-7, 11-14, and 18-21 is unwarranted and should be withdrawn.

Regarding new claims 23 and 25, and also independent claim 15, So fails to disclose first through P-th data buffers connected to the system data buses. Regarding new claims 22 and 24, So fails to disclose memory devices that share data pins with other memory devices.

Based on the following remarks, all of the now pending claims define over the teachings of So and the prior art taken as a whole. Accordingly, reconsideration and favorable action on claims 1-2, 5-9, 11-16, and 18-25 is respectfully requested.

Respectfully submitted,

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